

ABSTRACT

The present invention is a high speed serial memory interface system and method that facilitates efficient communication of information between a system controller operating at a relatively high speed serial communication rate and a memory array operating at a relatively slow speed serial communication rate. In one embodiment the present invention is a high speed serial memory interface system with an information configuration core for coordinating proper alignment of information communication signals, a system interface for communicating with a system controller, and a memory array interface for communicating with a memory array. A memory module array for storing information and a high speed serial memory interface system for providing interface configuration management are integrated on a single substrate.

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